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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,134	11/15/2001	Linden Minnick	042390P12310	6022

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EXAMINER	
TRUONG, LECHI	

ART UNIT	PAPER NUMBER
2194	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,134	MINNICK ET AL.	
	Examiner	Art Unit	
	LeChi Truong	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-12 and 14-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-12 and 14-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-11, 12, 14-22, 23, 25-27, 28, and 30-32 are presented for examination. Claims 2, 13, 24, 29 are cancelled.

Claim Objections

2. Claims 3-4, 11, 14-16 are objected to because of the following informalities: Claims 3-4, 11 depended on claim 2, claims 14-16 depended on claim 13 but claims 2 and 13 are canceled. Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-11 are rejected under 35 U.S.C. 101 because they are directed to non-statutory subject matter.

4. Claim 1 is directed to method steps, which appear to be abstraction, therefore they are directed to non-statutory subject matter. Specifically, as claimed, it is uncertain what performs each of the claimed method steps. The claimed steps to not define the machine of computer implemented process and therefore, they are abstraction.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claims 1-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lack proper antecedent basis:

The completion status – claims 1, 12, 23, 28 ;

6. Claims 1-28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As to claims 1, 12, 23, 28, " command includes a command, a memory address identifying a memory location to which the complete status will be written, and value to be written upon completion of the command" was not described in the specification. The specification (page 7, ln 25-28 and page 8, ln 21-25) describes an operation descriptor which includes, among other things, the command itself, a value to be written upon completion of the command, and a memory address which pointer to or identifies a memory location to which the command's completion indication is to be written/ As each command is completed, its completion status is written to the memory location includes in the operational descriptor that contain the command.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, **12, 23, 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) and further in view of Uchishiba et al (US. Patent 5,315,500).

As to claim 1, Harrington teaches the invention substantially as claimed including: a plurality of commands (list of command sequences, col 2, ln 15-20), a controller (I/O controller, col 2, ln 15-20), issuing a plurality of commands to a controller, wherein the commands are issued in a first order (col 2, ln 15-20), the completion status of commands is indicated in a second order (col 2, ln 20-25, col 4, ln 50-55), the term the second order is capable of being different from the first order (col 2, ln 22-25/ ln 26-30/ col 12, ln 3-10), issuing commands (issuing a PIO command, col 12, ln 5-10), includes command (the register 14 A and 14 B contain the command arguments while register C contains the command code, col 11, ln 30-35).

Harrington do not explicitly teach include a memory address identifying a memory location to which the completion status will be written, a value to be written upon completion of the command. However, Uchishiba teaches include a memory address identifying a memory

location to which the completion status will be written, a value to be written upon completion of the command (memory means 150, and the output address of the operational commands, input address of the signals representing the completion of the operations ... status flag 230 are inverted, for example from "0" to "1" when the signal representing the completion of the operation is received by a PC corresponding to the operation command, col 2, ln 35-45/ Fig. 2).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Harrington and Uchishiba because Uchishiba's include a command, a memory address identifying a memory location to which the completion status will be written, a value to be written upon completion of the command would improve the efficiency of Harrington's system by providing great flexibility for modification of control logic programmed in PC by identification of logical addresses during a series of sequential control proceedings.

As to claim 12, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above. In additional, Harrington teaches a machine –readable medium having instruction (col 3, ln 10-15).

As to claim 23, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above.

As to claim 28, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above. In additional, Harrington teaches a plurality of computation units (col 4, ln 6-9).

8. Claims **5, 11, 13, 16, 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) and further in view of Uchishiba et al (US. Patent 5,315,500), as applied to claim 1 above, and further in view of Fischer (US. Patent 4,783730).

As to claim 5, Harrington and Uchishiba do not teach each command is stored in a first memory location, the complete status is written to a second memory location different form the first memory location. However, Fischer teaches each command is stored in a first memory location, the complete status is written to a second memory location different form the first memory location (the command /status Doubleword 50 is a 32 bit entity that is divided into two 15 bit words. The high order word bits 16-31 contain status information. The low order word bits 0 to 15 include command information, col 8, ln 65-68 to col 9, ln 1-5/ the recipient thereafter perform the command and reports the successful completion of the command or an error condition upon attempting to execute that command. This reporting on the status of the command is written into the higher order word of the Command/ Status Doubleword, col 9, and ln 14-20).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Harrington and Uchishiba because Uchishiba's the complete status is written to a second memory location different form the first memory location would improve the efficiency of Harrington's system by providing great flexibility for modification of control logic programmed in PC by identification of logical addresses during a series of sequential control proceedings.

As to claim 11, Harrington teaches the value to be written indicated the command's original location (col 11, ln 60-65).

As to claims 13, 16, 17, they are apparatus claims of claims 11, 5; therefore, they are rejected for the same reasons as claims 11, 5 above.

9. Claims **3, 4, 14, 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) in view of Uchishiba et al (US. Patent 5,315,500), as applied to claim 1 above, in view of Fischer (US. Patent 4,783730) and further in view of Kohn (US. Patent 4,366,536).

As to claims 3, 4, Harrington, Uchishiba and Fischer do not teach an absolute address and an offset from a base memory address. However, Kohn teaches an absolute address and an offset from a base memory address (address indicated the offset, the absolute variable data are addresses, col 2, ln 8-16/ ln 42-45).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Harrington, Uchishiba, Fischer and Kohn because Kohn's address indicated the offset, the absolute variable data are addresses would improve the efficiency of Harrington, Harrington and Uchishiba's systems by providing addresses to the respective memories and the program counter to the respective memories to make the i/o system more consistant.

As to claims 14, 15, they are apparatus claims of claims 3, 4; therefore, they are rejected for the same reasons as claims 3, 4 above.

10. Claims **6-9, 18-21, 25-26, 30-31** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) in view of Uchishiba et al (US. Patent 5,315,500), as applied to claim 1 above, and further in view of Saito (US. Patent 6,567,862 B1).

As to claim 6, Harrington and Uchishiba do not teach the commands are grouped into categories. However, Saito teaches the commands are grouped into categories (groups received commands and stored commends to predetermined command group are according to group, col 2, ln 28-35).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Harrington, Uchishiba and Saito because Saito's groups received commands and stored commends to predetermined command group are according to group would improve the flexibility of Harrington, Uchishiba 's systems by allowing movement of a recording head of the data server to be reduced. Therefore, the efficiency of disk access could be improved.

As to claims 7, 8, 9, Saito teaches their execution time/ a plurality of resource executes / a plurality of memory location (according to a recording area on the data recording medium accessed by each command, col 3, ln 1-5/based on this address information... corresponding to the access disk, col 8, ln 45-56/ at the command execution time T', col 12, ln 41-42).

As to claims 18-21, 25-26, 30-31, they are apparatus claims of claims 6-9; therefore, they are rejected for the same reasons as claims 6-9 above.

10. Claims **10, 22, 27, 32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) of Uchishiba et al (US. Patent 5,315,500), as applied to claim 1 above, in view of Saito (US. Patent 6,567,862 B1) and further in view of Ghaffari et al (US. Patent 6,088,740).

As to claim 10, Harrington, Uchishiba and Saito do not teaches a single memory location. However, Ghaffari teaches a single memory location (a set of n command blocks 210-211, col 4, ln 4-10).

I would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Harrington, Uchisiba, Saito and Ghaffari because Ghaffari's a single memory location improve the reliability of Harrington, Uchishiba, Saito 's systems by executing discrete commands quickly and efficiently for an error recovery when necessary.

As to claims 22,27, 32, they are apparatus claims of claim 10; therefore, they are rejected for the same reason as claim 10 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LeChi Truong whose telephone number is (571) 272 3767. The examiner can normally be reached on 8 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomson, William can be reached on (571) 272 3718. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR of Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

LeChi Truong

May 1, 2006

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER